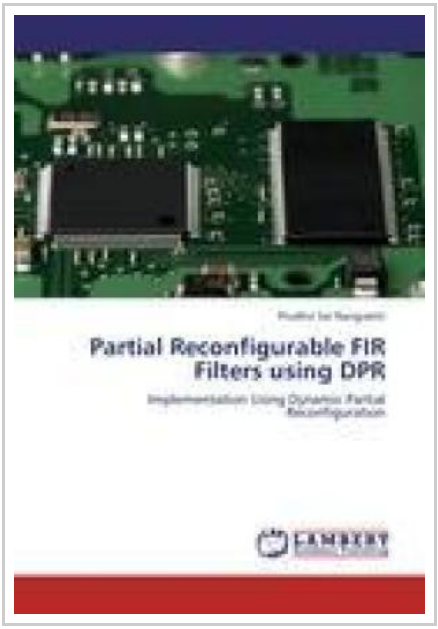

Partial Reconfigurable FIR Filters using DPR

By Prudhvi Sai Rangisetti

LAP Lambert Academic Publishing Dez 2014, 2014. Taschenbuch. Book Condition: Neu. 220x150x6 mm. This item is printed on demand - Print on Demand Neuware - Reconfigurable hardware might be the next step which will give computer performance a new big leap forward. The idea is to use the, nowadays, high performance FPGA technology to adapt the hardware to the problem. Dynamic partial reconfiguration of FPGA offers new design space with variety of benefits. This Dissertion intends to describe the development of a dynamically reconfigurable system which supports multiple modules running concurrently, all with hardware support. A standard Xilinx FPGA is used to test the possibilities of loading partially new hardware configurations while other parts of the FPGA still are active. An example implementation is also realized in order to exemplify the possibilities within the subject. Its scope is to implement an autonomously reconfigurable digital signal processing architecture that is tailored for the realization of arbitrary response FIR filters and flexibility allowing dynamically inserting and/or removing the partial reconfigurable FIR filters with various taps. 96 pp. Englisch.

Reviews

Completely essential read publication. I am quite late in start reading this one, but better then never. You wont truly feel monotony at at any moment of your time (that's what catalogs are for regarding should you question me).

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